AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (cancelled)

4. (previously presented) A data processing device formed as a semiconductor integrated circuit to be coupled to an external memory device for performing data transmission and reception, said data processing device comprising:

a central processing unit;

a clock pulse generation circuit capable of generating different clock pulse signals; and

an interface unit for data transmission and reception to and from the external memory device,

wherein said interface unit includes:

an external clock output terminal for outputting a clock signal derived from a clock pulse signal generated by the clock pulse generation circuit;

an output driver for driving said external clock output terminal to output said clock signal;

a load circuit capable of imparting, to the clock signal extracted from a position in a stage previous to said output driver in a clock signal path, a variable delay in accordance with a delay resulting from an external load coupled to said external clock output terminal;

a plurality of external data input terminals for receiving data from the external memory device; and

a plurality of latch circuits for latching data received by said plurality of external data input terminals,

wherein said latch circuits latch data based on the clock signal as delayed by said load circuit.

Claims 5-6 (cancelled)

7. (previously presented) A data processing device according to claim 4, wherein said load circuit includes a time constant circuit comprising resistors and capacitors.

8. (previously presented) A data processing device according to claim 4,

wherein said load circuit includes a plurality of time constant circuits, generates a plurality of clock signals with different amounts of delay, and selects any of the

plurality of clock signals for latching data inputted from the external memory device.

9. (previously presented) A data processing device according to claim 8, wherein said load circuit includes:

a selector circuit which selects a signal passing through or not passing through any of the plurality of time constant circuits as the clock signal for latching data inputted from the external memory device.

10. (previously presented) A data processing device according to claim 9, further comprising:

a register which stores a set value for determining a state of said selector circuit; and

a decoder which generates a control signal for said selector circuit in accordance with the set value of the register.

Claims 11-12 (cancelled)

13. (previously presented) A data processing device according to claim 4, wherein said load circuit extracts the clock signal from a stage immediately preceding said output driver.